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Simulation and performance analysis of simplified multilevel inverter

Rahul V A[1], Sheryl Grace Colaco[2]

PG student, Department of E&E, St.Joseph engineering college, Mangalore, India [1]

Professor, Department of E&E, St.Joseph engineering college, Mangalore, India [2]

Abstract: Multilevel converters are widely used due to its high efficiency, low harmonics and also its output waveform is almost similar to sinusoidal shape. There are many topologies developed for multilevel converter each of them has various advantages and disadvantages. In this paper a new topology is proposed which is a combination of conventional multilevel topology and H-bridge circuit having advantages of both. Here a 7 level multilevel inverter derived from the proposed topology is explained for analysis.

Keywords: Multi-level converter, 7 level inverter, gate drive circuit, charge pump circuit.

I. INTRODUCTION

There are many topologies have been introduced based on multilevel concept. They can be listed as Diode clamped multilevel inverter, Capacitor clamped multilevel inverter [1], [2], [3], and also other topologies [4]. Each of which have certain advantages and disadvantages. The proposed topology is compared with other existing topologies in terms of number of switches used and the blocking voltage (maximum Drain-Source voltage) required for each switch. These topologies are also compared in terms of number of capacitors, number of switches, number of diodes used in the circuit, the maximum blocking voltage requirement across each switch, and the peak to peak output voltage. Comparing all these topologies it is found that the proposed topology is having certain advantages over other topologies while considering the number of switches and maximum blocking voltage requirement across each switch.

Some of the advantages of proposed topology are less switching loss due to reduced number of components and simplified circuit compared with other topologies.

II. NEW MULTILEVEL INVERTER TOPOLOGY

A new multilevel topology is proposed, it is a combination of H-bridge circuit and neutral point clamped multilevel inverter. The advantage of conventional neutral point clamped multilevel is that the blocking voltage across all switching elements are same and of minimum magnitude. There are new topologies introduced with lesser number of switching components but each switching component should have a blocking potential of magnitude equal to DC bus voltage. In this proposed topology one side of H-bridge is similar to conventional diode clamped multilevel inverter and the other side is just to switch between 0V and V_{DC} bus voltage. So that except two switching components all other switching components have to block only a voltage of less magnitude. Here, a 7-level inverter is explained with 8 switching elements. Six of them should have maximum drain to source voltage of magnitude equal to $1/3^{rd}$ of V_{DC} and the other two equal to V_{DC} bus voltage.

Fig.1 shows the output waveform of proposed inverter. The applied DC bus voltage is 24V. The three DC link capacitors divide the voltage equally across them. The voltage between each switching steps is 8V. A resistive load is connected for the experimental setup to verify the working of the topology.

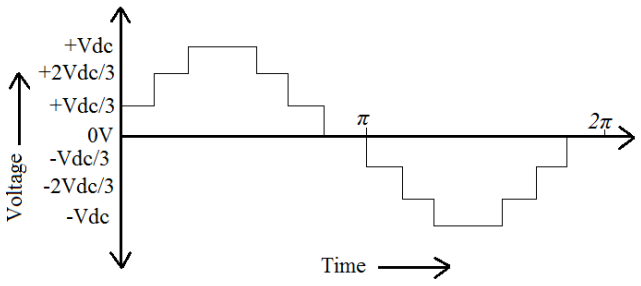

Fig.1 Output waveform for one cycle of operation

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Operations of proposed inverter topology

The circuit diagram is shown in Fig.2. There should be seven voltage levels in the output waveform to approximate its fundamental to a sinusoidal voltage. The seven voltage levels are obtained by using DC link capacitors and they are +Vdc/3, +2Vdc/3, +Vdc, 0V , –Vdc/3, –2Vdc/3 and –Vdc. There should be a switching sequence for obtaining these voltage levels. Different voltage levels and their switching combinations are shown in Table 1. The switches are turned on or off according to the above table using a suitable delay and also by keeping the time period of 0.02ms which is equal to a frequency of 50Hz. For the easiness of explanation DC link capacitors are replaced with voltage sources V1, V2, V3 and their magnitude is assumed as 8V.

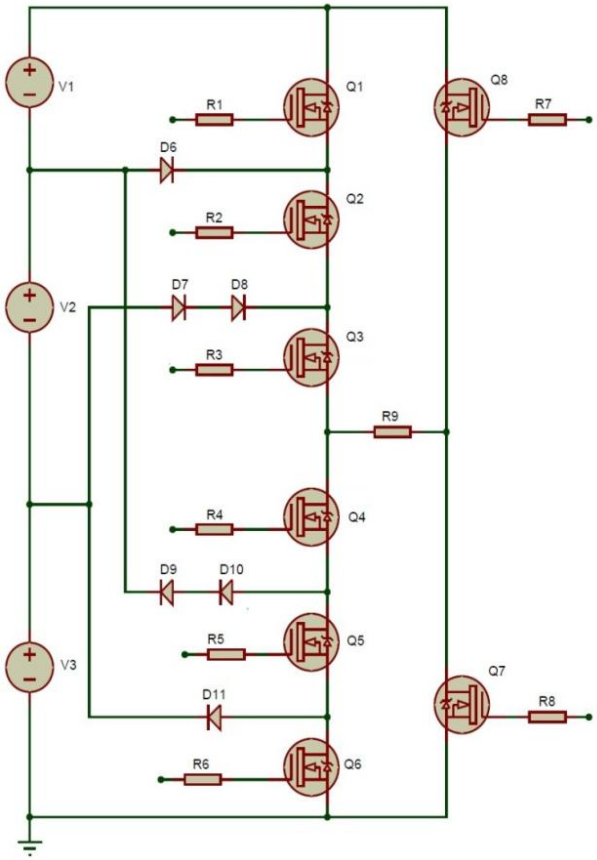

Fig.2 Proposed inverter topology

Sl. No.	Voltage level	SWITCHES							
		Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
1	$+V_{dc}/3$	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
2	$+2V_{dc}/3$	OFF	ON	ON	OFF	OFF	OFF	ON	OFF
3	$+V_{dc}$	ON	ON	ON	OFF	OFF	OFF	ON	OFF
4	$-V_{dc}/3$	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON
5	$-2V_{dc}/3$	OFF	OFF	OFF	OFF	ON	ON	OFF	ON
6	$-V_{dc}$	OFF	OFF	OFF	ON	ON	ON	OFF	ON
7	0V	ON	ON	ON	OFF	OFF	OFF	ON	OFF
		OFF	OFF	OFF	ON	ON	ON	OFF	ON

Table.1 Comparison of different multilevel topologies

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a) Output voltage : +Vdc/3(8V)
For an output step voltage $+V_{dc}/3$ the MOSFETs Q3 and Q7 must be turned on. The current flows in the direction V3, D7, D8, Q3, R9 (load resistor) and Q7.

b) Output voltage : +2Vdc/3
To obtain an output step voltage $+2V_{dc}/3$ the MOSFETs Q2, Q3 and Q7 must be turned on. The current flows in the direction V3, V2, D6,Q2, Q3, R9 (load resistor) and Q7.

c) Output voltage : +Vdc
To obtain an output step voltage $+V_{dc}$ the MOSFETs Q1, Q2, Q3 and Q7 must be turned on. The current flows in the direction V3, V2, V1, Q1, Q2, Q3, R9 (load resistor) and Q7.

d) Output voltage : -Vdc/3
For an output step voltage $-V_{dc}/3$ the MOSFETs Q8 and Q4 must be turned on. The current flows in the direction V1, Q8, R9 (load resistor), Q4 and D10, D9.

e) Output voltage : -2Vdc/3
For an output step voltage $-2V_{dc}/3$ the MOSFETs Q8 and Q4, Q5 must be turned on. The current flows in the direction V1, Q8, R9 (load resistor), Q4, Q5, D10 and V2.

f) Output voltage : -Vdc
For an output step voltage $-V_{dc}$ the MOSFETs Q8 and Q4, Q5, Q6 must be turned on. The current it flows in the direction V2, V1, Q8, R9 (load resistor), Q4, Q5, Q6 and V3.

g) Output voltage : 0V
0V can be obtained in two ways. One method is turning MOSFETs Q4, Q5, Q6 and Q7 on at the time so that both the terminals of R9, load resistor, are at same ground potential. The second method is turning MOSFETs Q1, Q2, Q3 and Q8 on at the time so that both the terminals of R9 are at same potential.

III. SIMULATION AND ANALYSIS

The simulation of proposed 7-level inverter topology is performed in Matlab for output waveform and Fast Fourier Transform (FFT) analysis.

Input DC Voltage : 24V
DC link Capacitors : 4000uF
Diodes : Diode
MOSFET : N-channel
Load :50Ω Resistor
Pulse to gate : Pulse Generator
Output Frequency : 50Hz.

Three Dc link capacitors of 4000uF are used to divide the 24V to 8V (step voltage)[5]. The MOSFETs Q7 and Q8 are driven with pulse generators of periods 0.02ms. All other switches are driven with a period of 0.01ms. The output waveform is shown in Fig.3. The timing of pulse is adjusted to get minimum harmonics[6]. From the waveform it is seen that the out voltage is switches between +24 and -24. The frequency is 50Hz. Fig.4 also shows the output voltage and switching pulse to each switch.

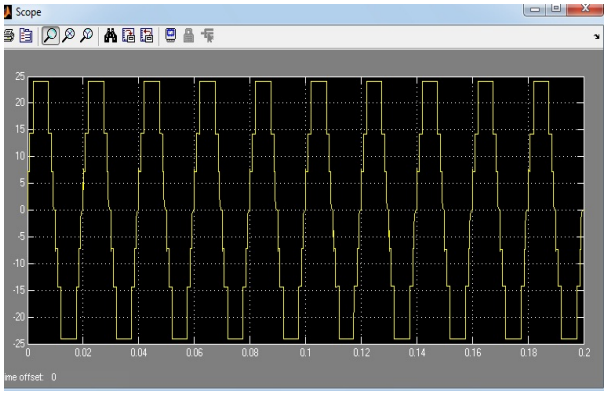

Fig.3 7 level inverter output waveform in Scope

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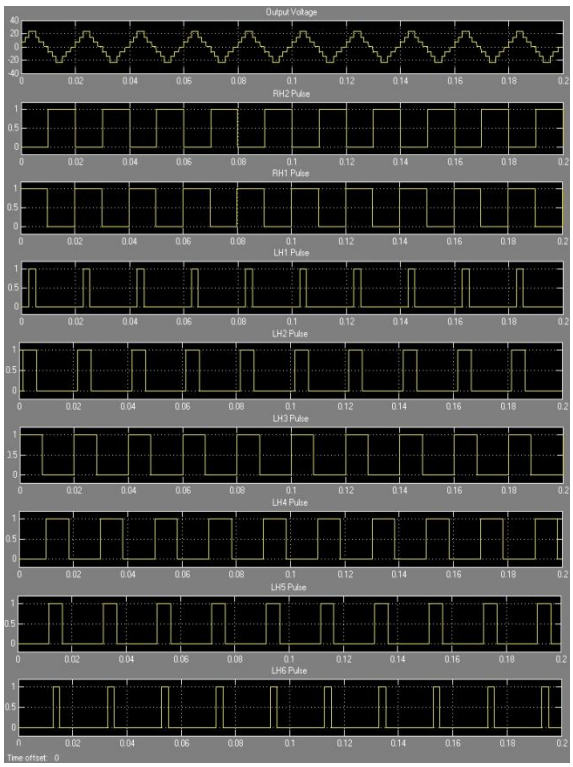

Fig.4 Output voltage waveform and switching pulse to each switch

The voltage across the DC link capacitor has to be maintained constant. The Fig.5 shows the voltage across the capacitor and the output voltage measured by multimeter. The DC link voltage is a constant at 8V. And the peak to peak output voltage is 48V. The MOSFETs Q7 and Q8 connect the output to ground and 24V respectively. The other switches are pulsed accordingly to a get a stepped wave whose fundamental is similar to sine wave. RH1 and RH2 are on once in a cycle and all other switches are turned on twice in a cycle.

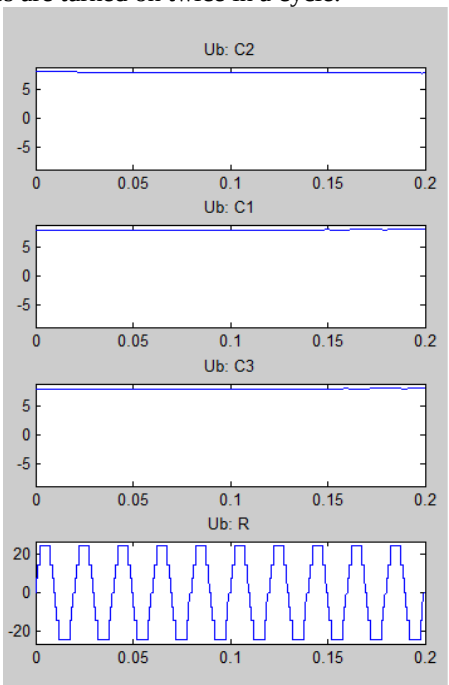

Fig.5 DC link voltage and output voltage waveform measured using Multimeter

The FFT analysis is shown in Fig.6. The fundamental output voltage is 26.95 and the Total harmonic distortion [7] is 13.56%.

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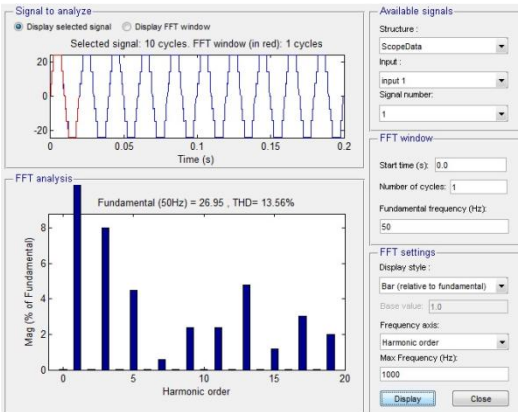

Fig.6 DC link voltage and output voltage waveform measured using Multimeter

IV. PROTEUS SIMULATION

The advantage of Proteus is that the entire circuit can be simulated in component level. The simulation can be performed from the concept to the completion. Here the simulation is done including the inverter topology, gate drive circuit and controller. The HEX code is loaded to the controller to generate pulses. For driving the gate MOS gate driver IC is used. Instead of DC link capacitors three DC voltage sources of 8V is used. Arduino Uno is used as the controller to drive the MOSFET switches. Arduino has sufficient PWM signal pins to drive the switches and it is easy to program. The output waveform shown in Fig.7 shows that the peak to peak voltage is 48V and the frequency is 50Hz (Time period=20mS).

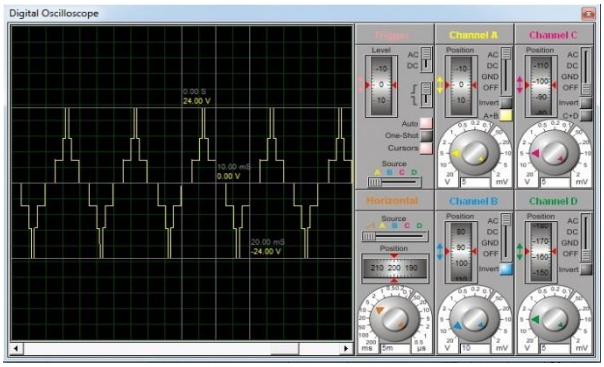

Fig.7 Output voltage waveform in Proteus

V. CONCLUSION

This paper presented simulation and performance analysis of new multilevel inverter topology. The topology is simulated in Matlab for analysis and the overall circuit is simulated in Proteus for verification. The THD, Harmonic factor, and Distortion factor are calculated theoretically and practically. And the circuit with MOSFET gate drivers is simulated in Proteus and the output is verified. The proposed topology can be used in medium and high power application.

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